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Beacon Initiated Reconfigurable SDR Controller on FPGA for High Speed Communication System

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ABSTRACT: Wireless sensor network (WSN) is widely used network all over the world. They are very useful and easy to implement. WSN receiver initiated Duty-Cycle asynchronous MAC protocols have been proposed now a days. The radio which is used to measure and detect the signal strength of radio signal which is transmitted by radio. Satellite beacon signal are always low power signals for power control. Beacon signals can be used for measurement due to their power and frequency. This type of MAC protocol can be used for Burst traffic & many other applications.

In this we can reduce end to end packet delivery & Power consumption for various data rates. End to end packet delivery and Power consumption for burst traffic and many other applications can be reduced by adjusting beacon time of receiver. We can also adjust listening time of sender according to beacon time.

KEYWORDS: Wireless sensor networks, Receiver initiated, Duty cycle, Energy-efficient Low latency Energy-efficient.

I. INTRODUCTION

Energy consumption plays main role in wireless sensor network because we are unable to recharge or replace battery of each sensor node every time. Therefore duty cycle technique is used by MAC protocol in wireless sensor network for energy saving to on and off the device continuously. Propagation research basically depends on measurement of beacon receiver with other facts like readings of radio as well as weather conditions.

Synchronization of time is one of the important concepts to overcome message overhead and if time synchronization is not good then it may cause the problems like complexity in device and because of which device may become expensive. Duty cycle MAC protocols are of mainly two types; Synchronous and Asynchronous. In case of synchronous duty cycle MAC protocol wake up & sleeping time of sensor node are generally same. Asynchronous MAC protocol waking and sleeping time of sender is totally different. Energy consumption is reduced by duty cycle technique. Event detection can also be achieved by using beacon processor. Digital signal processing and software defined radio are nothing but applications of beacon receiver. Collision can be avoided in asynchronous MAC protocol using duty cycle technique by adjusting the beacon time of receiver. The problems such as performance degradation are always occurred in case of asynchronous MAC protocols using duty cycle technique. Cost and Performance of asynchronous duty cycle MAC protocol plays a vital role in case of wireless sensor network.

In this paper it can easily forward the Packet and also can achieve end to end packet delivery by adjusting the beacon time of receiver. Sender adjusts its listening time according to beacon time of receiver which can reduce the power consumption as well as idle listening. In this we can see how we can manage controlling of single hop latency with the help of end to end packet delivery. Sleep latency problem always occurs because when the data arrives the next sensor node may be in sleeping state. The sensor nodes continuously send the data packets along with burst. This fact cannot

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be used for some real time applications. Time synchronization is not necessary in case of asynchronous duty cycle MAC protocol using duty cycle technique because waking time and sleeping time of receiver are totally different.

II. RELATED WORK

The concept of receiver-initiated transmission in a MAC protocol is common, but we make the first effort to combine this conceptorganized with duty cycling in the perspective of MAC protocols. Contentiongrounded duty-cycle MAC protocols in WSNs can be categorized in two categories such as synchronous and asynchronous. MAC protocols, such as SMAC and T-MAC, or RMAC, or DWMAC and PRMAC, have necessity of the adjacent nodes to synchronize for communication to each other. In compare, MAC protocols, such as BMAC, or WiseMA, and XMAC, or RI-MAC and PW-MAC are asynchronous duty-cycle, and they do not need any synchronization between the adjacent nodes. The projectedMAC is an asynchronous duty-cycle MAC protocol, so we concentrate on asynchronous MAC protocols in this segment. In these current asynchronous duty-cycle MAC protocols, every node wakes up arbitrarily always. This arbitrary wakeup announcesadditional packet transfer latency. Mainly for gust traffic, they suffer from severe performance deprivation. Moreover, as because of the sender doesn't know the receiver wake up time in some MAC protocols (e.g. BMAC, or XMAC and RI-\ MAC), it has to instantly wake up when it wishes to transmit data packets, which trashes a abundant deal of energy.

In RI-MAC, as shown in below Fig. 1, when a packet reaches at a sender, it get wakes up and just waits for a base beacon from its proposed receiver. As the receiver wakes up, it directs a base beacon as an invitation for data communication. When the sender accepts the beacon dispatch then the datacommunication will twitchWhen the data is magnificentlyacknowledged, the receiver shows a beacon as an acknowledgement (similarly used as an invitation for fresh data communication). If aaccident occurs, the receiver propels a beacon which comprises the backoff window size.

III. PROPOSED WORK

The idea of beacon Initiated reconfigurable SDR controller on FPGA for high speed communication system is not new but we add duty cycle technique here which helps us to reduce the power consumption and increases the efficiency of that protocol. When the data packets arrives at the sender it wakes and wait for beacon signal from its receiver i.e in other word we can say it invites receiver for data transmission. When beacon signal is received by sender the data transmission actually start and when all data will successfully sent receiver also send the beacon signal as an acknowledgement which we can say new invitation for transmission of data.

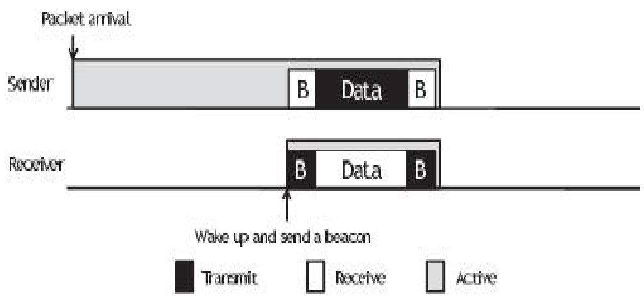

Fig 1.Operation of RI-MAC

In this way each node wakes up randomly for continuously supervising the beacon signal which tells us that it is always ready to receive the data. when the sensor node has so many data packets waiting in a queue then sensor node transmit the data one by one immediately but if no any data packet is received then the sensor node will go to sleep mode and save the power consumption.

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In this proposed work, it is shown that design of transmitter and receiver for software defined radio. The main controller combines all signals of transmitter and receiver. The input signals for transmitter are clock, power gating, base beacon and data which we have to send. On the other hand the output signals are received data, radio status, and CRC. CRC is nothing but checksum which we have to add in the input data to crosscheck whether whatever data send by sender exactly we got at receiver or not! Acknowledgement is given by both sender as well as receiver. Similarly the input signals to receiver are clock, power gating and input data and at the output side beacon from transmitter memory to save the status of device. Device status tells us our device is on or off. Main controller combines input signals of transmitter to the receiver. There is one multiplier which filters out the output data. When supply is zero system is in ideal mode. When data arrives base beacon is send by sender to receiver and data transmission takes place. When data successfully received receiver also send the beacon signal.

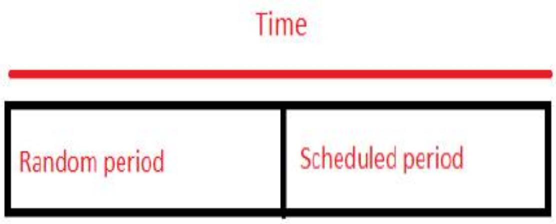

Fig 2.Timing Diagram

IV. HARDWARE AND SOFTWARE DESIGN

Both of these hardware and software are much precisely designed. Whenever the power supply is off the fsm is in idle state. When it becomes 1 sender sends the base beacon to receiver as invitation for transmission of data.

There are lot many things like device status, radio status. Power gating, Checksum i.e. CRC, multiplier unit for filtering out the data are there in this system. When power gating is one data transmission is successfully done while on the other hand when it is zero sender will not send any acknowledgement that is base beacon to receiver and transmission of data stops.

V. RESULT

Primarily, each node i is in Random period and selects its beacon time *Tibeacon* arbitrarily. Each node arbitrarily wakes up at its beacon time to inform that it is set to receive the data packets by broadcasting a beacon. Once the nodes sense the event it transfers the data packets to the sink node through multi-hop relaying. When sender S transfers the data packets to its receiver, S's succeeding beacon time TbeaconSis piggybacked into the data packet. Uponreceiver R accepts the data packets, R updates it's succeeding beacon time corresponding to S based on Tbeacon S.

$$T^{R}\text{beacon,S}=\text{Tbeacon,S}+\text{Tguard}$$

where*Tguard* can confirm that S receives all line up packets from its preceding hop.

Particularly, because R may have several senders, R should select minimum next beacon time as its scheduled next beacon time.

$$T^{R}_{beacon} = \min_i(T^{R}_{beacon,i} >= \text{TIME\_NOW}).$$

Case I:

The transmitter S is in RP now.*Tlisten,R*is set asthe time of the data arrival. It means that S starts to receive to the

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channel once the data packets arrival. This can promise that transmitter S doesn't slip the beacon of receiver R.

Case II:

S transmits the data packet to R magnificently.R will calculate its succeeding beacon time as

TRbeacon,S=Tbeacon,S+Tguard

S recognizes when R will wake up to send its following beacon so that it can plans its listening time at,

Tlisten,R = TRbeacon,S.

Case III:

As S doesn't obtain anydata packet at *TSbeacon*, so R too cannot accept anything at *TRbeacon,S*. Since both of S and R are in SP, R plan its next beacon time:

T beacon,S=T beacon,S+Tcycle

and S governs its next scheduled listening time:

$$T^{1}listen,R=Tlisten,R+Tcycle=T^{R}beacon,S+Tcycle.$$

Case IV:

R receives the data packet magnificently anddirects its ACK, but S doesn't obtain ACK from R.
R receives the data packet magnificently but not recognizes that S doesn't obtain ACK, so it computes its following beacon time based on *Tbeacon,S*piggybacked into the data packet:

Consequently, in order to guarantee that S and R can rendezvous, S should calculate its next scheduled listening time as:

$$T^{1}listen,R= min(Tlisten,R+ Tcycle,Tbeacon,S+ Tguard).$$

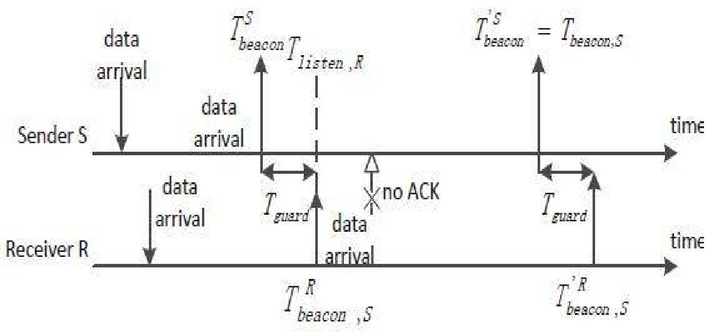

Fig. Case IV

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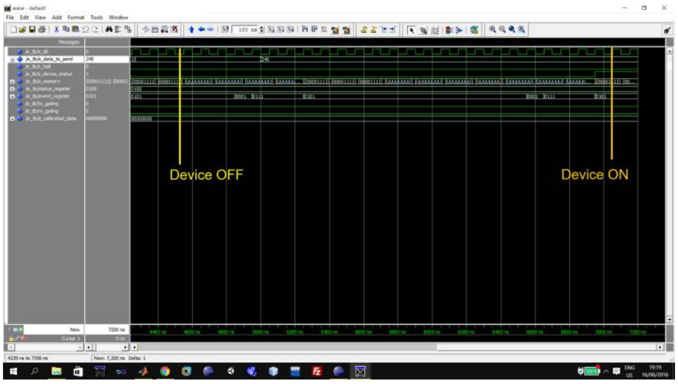

Fig. Simulation Result

VI. CONCLUSION AND FUTURE WORK

There are two advantages of platform combining DSP and FPGA. DSP accelerates hardware for FPGA. On the hand other as we know that FPGA already have partial reconfiguration capability because of which we can easily reduce the size of software which is downloaded. In this we have proposed a new Receiver Initiated Asynchronous MAC protocol having duty cycle technique for Burst Traffic.

This system improves the performance by reducing the end to end packet delivery which saves energy and also increases the life time of sensor nodes. In this E-controller can also added which can combines signals of both transmitter and receiver in software defined radio. So that power consumption can also be reduced on large scale because whenever the acknowledgement is not send or received by device data transmission stops and energy can be saved.

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